晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-240320AHTZQW-00
APPROVED BY	
DATE	

☐Approved For Specifications
☐Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2018/7/3	--	New Release	Kokai

1 Features

This display module is a color active matrix thin film transistor (TFT) liquid crystal display that uses amorphous silicon TFT as a switching device.
This TFT LCD panel has a 2.4 inch diagonally measured active display area with QVGA resolution (240 horizontal by 320 vertical pixels array). It is suitable for hand-held application. The LCD adopts one backlight with High brightness 4-lamps white LED.

(1) LCD: 1.1 Amorphous-TFT 2.4 inch display, transmissive, normally Black , IPS type.
1.2 240(RGB) X320 dots Matrix
1.3 LCD Driver IC: ILI9341V
1.4 Viewing Direction : All Direction.
(2) Compatible with ROHS Standard.

Mechanical specifications

Item	Specifications	unit
Display resolution(dot)	240(W) x 320(H)	dots
Active area	36.72(W) x 48.96(H)	mm
Pixel pitch	0.153 (W) x 0.153 (H)	mm
Pixel Arrangement	R.G.B -stripe	-
Overall dimension	43.6 W x 61.50 x 2.28	mm
Contrast ratio	800(typ)	-
Display Type	Transmissive	-
Display Mode	Normally Black	-
Brightness	250	Cd/m^2

2 Absolute max. ratings and environment

2.1 Absolute max. ratings

Item	Symbol	Min.	Max.	Unit.	Note
Power supply voltage	VCC	-0.3	4.6	V	GND=0
Analog Operating Voltage	VCI	-0.3	4.6	V	GND=0
Logic Signal Input Level	V1	-0.3	VCC+0.3	V	

2.2 Environment

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Top	-20	60	℃	-
Storage Temperature	Tst	-30	70	℃	

3 Electrical specifications

3.1 Electrical characteristics of LCM

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	VCC	-	2.5	2.8	3.3	V
Analog Operating Voltage	VCI		2.5	2.8	3.3	V
I/O Operating Voltage	IOVCC		1.65	2.8	3.3	V
High-level input voltage	V_{IH}	-	0.7* IOVCC	-	IOVCC	V
Low-level input voltage	V_{IL}	-	0	-	0.3* IOVCC	V

Note (1): HSYNC, VSYNC, DE, Digital Data

Note (2): Be sure to apply the power voltage as the power sequence spec.

Note (3): GND=0V

Note (4):

- Select the MCU interface mode

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
					Register/Content	GRAM
0	0	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	0	0	1	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	0	1	0	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	0	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
0	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
0	1	1	0	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
1	0	0	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1]
1	0	0	1	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10]
1	0	1	0	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
1	0	1	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SDI: In SDO: Out	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SDI: In SDO: Out	

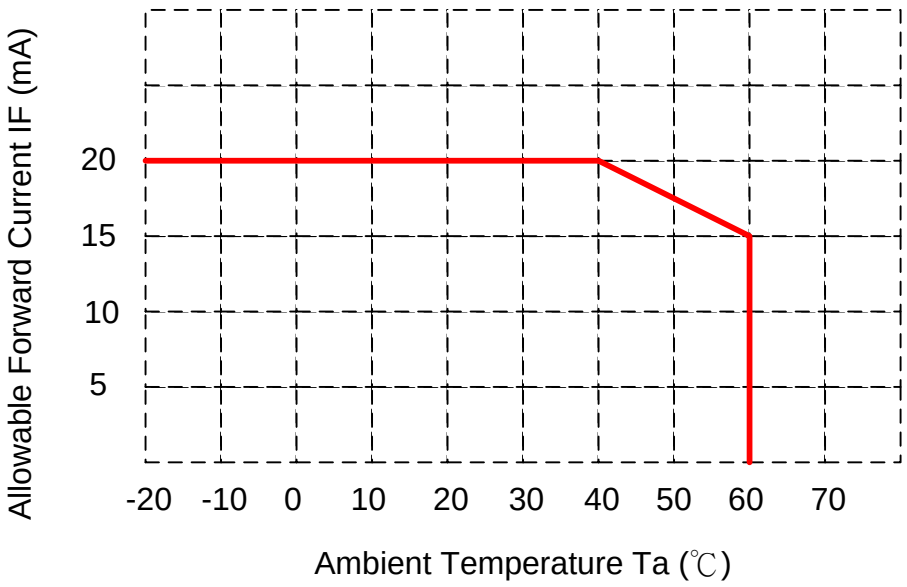
3.2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =20mA	2.8*4	3.2*4	3.6*4	V
Forward current	I_f	4-chip Serial	--	20	--	mA
Power Consumption	P_{BL}	I_f =20mA	-	256	-	mW
Uniformity (with L/G)	-	I_f=20mA	70%*1	-	-	-
LED Life time	-	I_f=20mA	50000	-	-	Hr
Luminous color	White					
Chip connection	4 chip Serial connection					

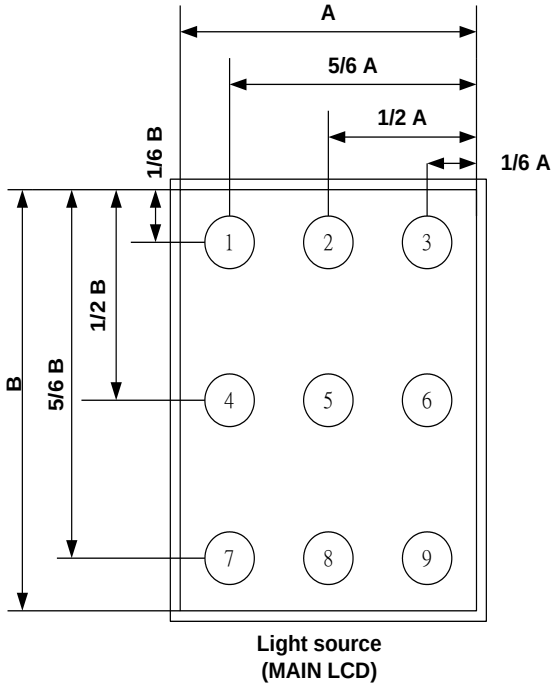
LED CIRCUIT DIAGRAM:

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Bare LED measure position:



*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 70\%$

4 Optical characteristics

Optical characteristics

Item		Symbol	Conditions	Min	Typ	Max	Unit	Note
Contrast Ratio		CR	Viewing normal angle $\Theta_x = \Theta_y = 0$	600	800	-	-	
Response Time		T_R+T_F		-	8	16	ms	(4)
Viewing Angle	Top	Θ_T	CR≧10	-	85	-	deg	(2)
	Bottom	Θ_B		-	85	-		
	Left	Θ_L		-	85	-		
	Right	Θ_R		-	85	-		
Module Chromaticity	Red	X_R	Viewing normal angle $\Theta_x = \Theta_y = 0$	Typ-0.05	0.606	Typ+0.05	-	-
		Y_R			0.364			
	Green	X_G			0.307			
		Y_G			0.569			
	Blue	X_B			0.142			
		Y_B			0.092			
	White	X_W			0.303			
		Y_W			0.325			
Brightness		-	LCD center	200	250	-	Cd/㎡	(1)

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25℃) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

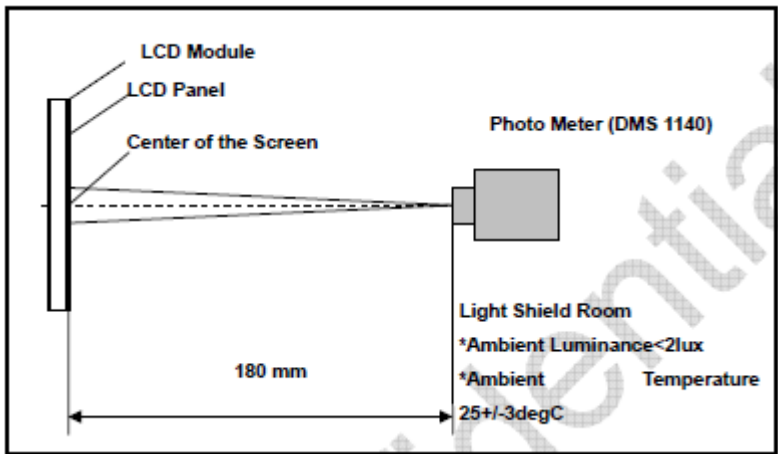


Figure 2 Measurement Setup

Note (2) Definition of Viewing Angle

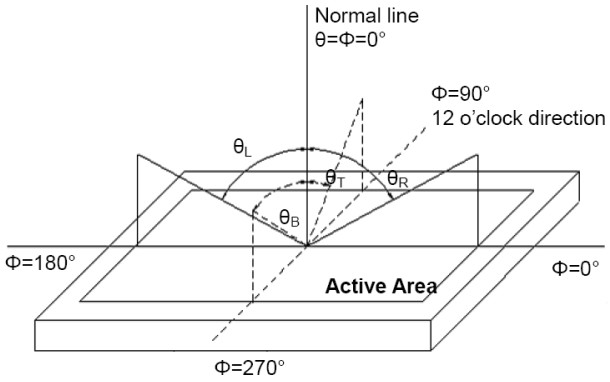


Figure 3 Definition of Viewing Angle

Note (3) Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition Of Response Time

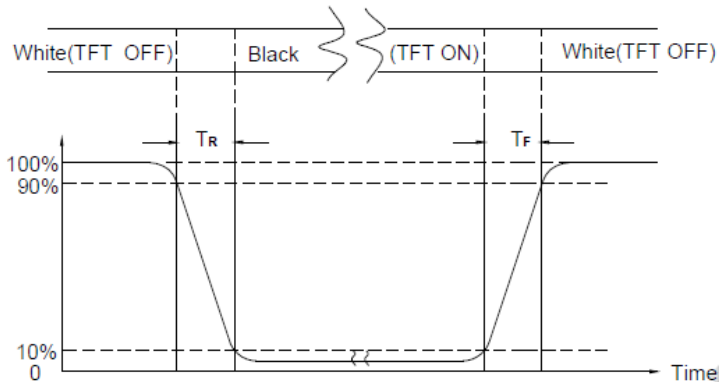


Figure 4 Definition of Response Time

6. Electrical Specifications

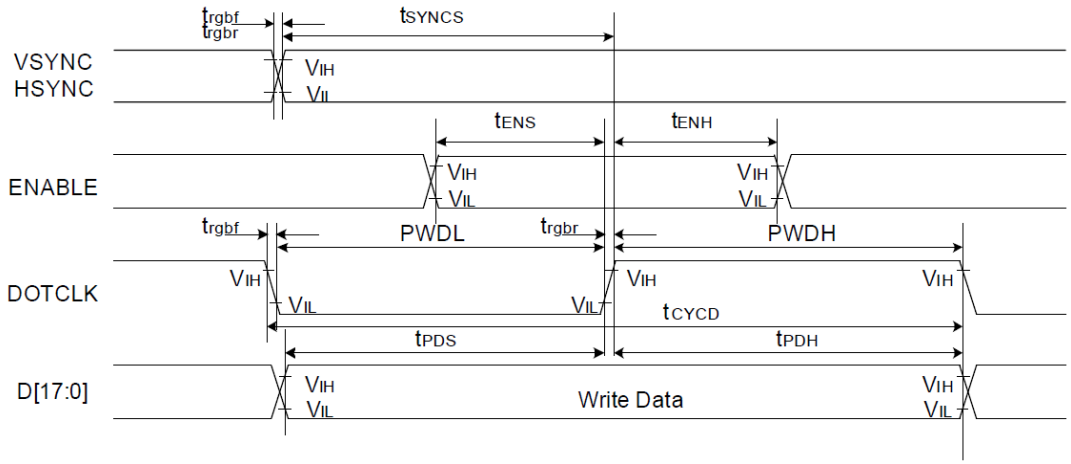
6.1 TFT LCD Panel FPC Descriptions

No.	Symbol	I/O	Description
1	GND	P	Power Ground
2	IM0	I	Select the MCU interface mode See Page 5
3	IM3	I	
4	IM2	I	
5	IM1	I	
6	RESET	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
7	VSYNC	I	-Vertical (Frame) synchronizing input signal for RGB interface operation. -If not used, please fix to the VCC or GND.
8	HSYNC	I	-Horizontal (Line) synchronizing input signal for RGB interface operation. -If not used, please fix this pin at VCC or GND.
9	DOTCLK	I	-Dot clock signal for RGB interface operation. -If not used, please fix this pin at VCC or GND.
10	ENABLE	I	-Data enable signal for RGB interface operation. -If not used, please fix this pin at VCC or GND.
11	DB17	I/O	Data input
12	DB16	I/O	Data input
13	DB15	I/O	Data input
14	DB14	I/O	Data input
15	DB13	I/O	Data input
16	DB12	I/O	Data input
17	DB11	I/O	Data input
18	DB10	I/O	Data input
19	DB9	I/O	Data input
20	DB8	I/O	Data input
21	DB7	I/O	Data input
22	DB6	I/O	Data input
23	DB5	I/O	Data input
24	DB4	I/O	Data input
25	DB3	I/O	Data input
26	DB2	I/O	Data input
27	DB1	I/O	Data input
28	DB0	I/O	Data input
29	SDO	I	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin

No.	Symbol	I/O	Description
30	SDI	I	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCC or GND.
31	RD	I	8080-I /8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VCC level when not in use.
32	WR	I	(WRX) - 8080-I /8080-II system: Serves as a write signal and writes data at the rising edge. (D/CX) - 4-line system: Serves as the selector of command or parameter. Fix to VCC level when not in use.
33	RS/SCL	I	(D/CX): This pin is used to select “Data or Command” in the parallel interface. When DCX = 1, data is selected. When DCX = 0, command is selected. (SCL): This pin is used as the serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface. If not used, this pin should be connected to VCC or GND.
34	CS	I	-Chip selection pin Low enable. High disable.
35	FMARK	O	Tearing effect output pin to synchronize MPU to frame writing If not used, open this pin.
36	IOVCC	P	I/O Power Supply
37	VCC	P	Logic Power Supply voltage
38	VCI	P	Analog Power Supply voltage
39	PWM_OUT	O	Output pin for PWM signal of LED driver.
40	LED_A	P	Backlight LED Anode.
41	LED_A	P	Backlight LED Anode.
42	LED_K	P	Backlight LED Cathode.
43	LED_K	P	Backlight LED Cathode.
44	NC	-	No connection.
45	GND	P	Power Ground

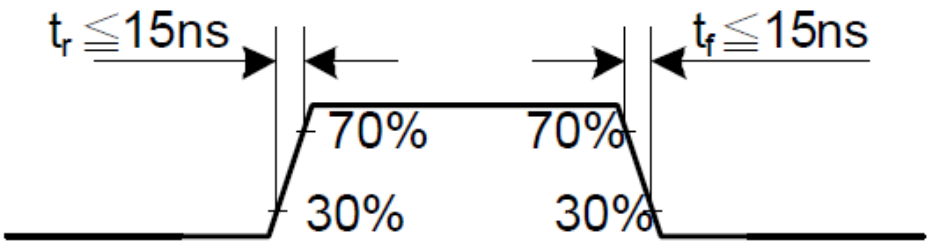
7 Timing

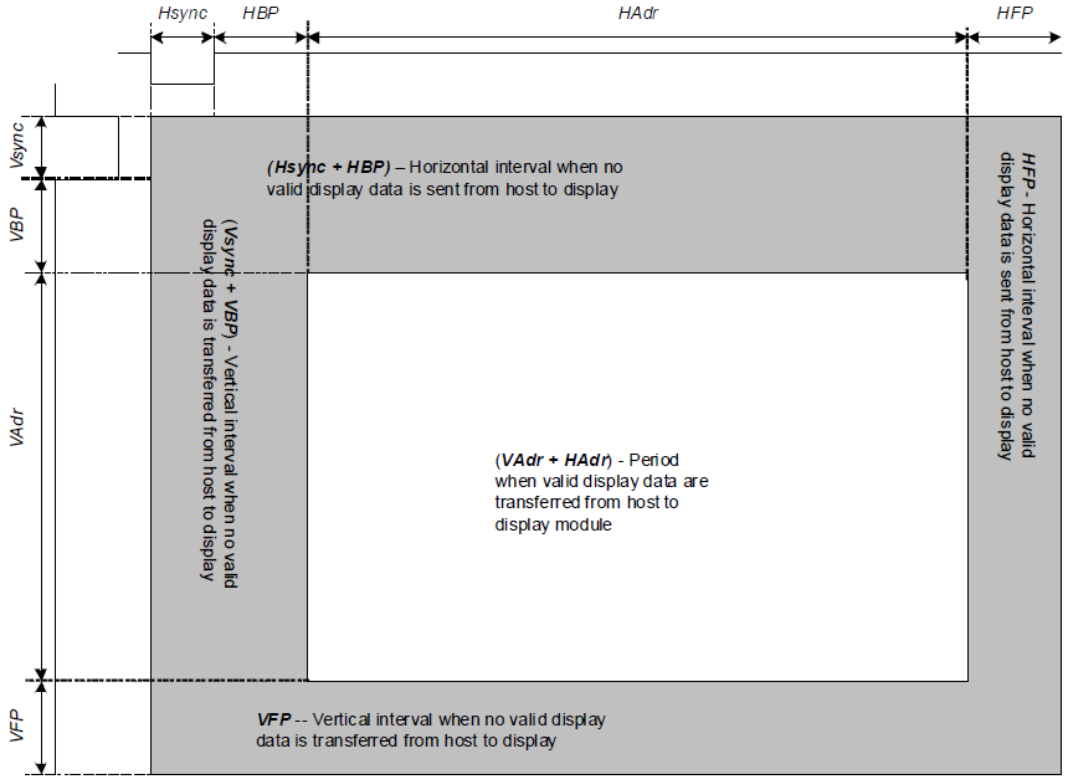
7.1 Parallel 18/16/6-bit RGB Interface



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

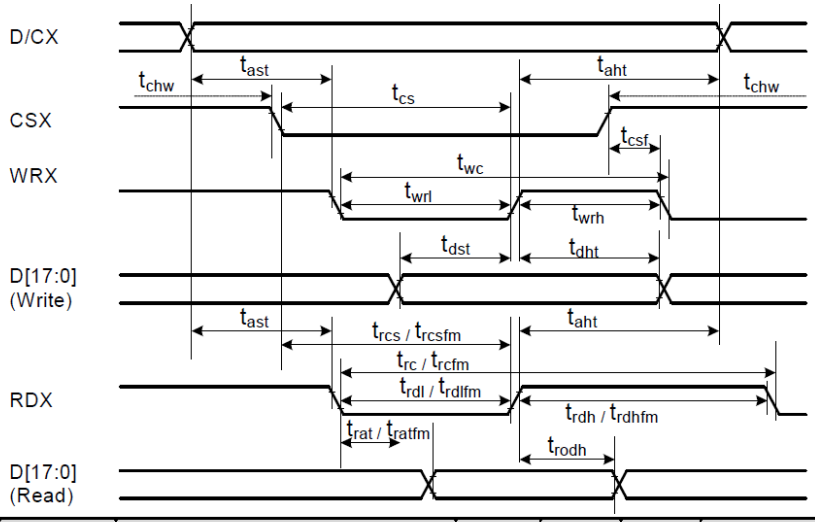
Note: VCC=2.5 to 3.3V, GND=0V





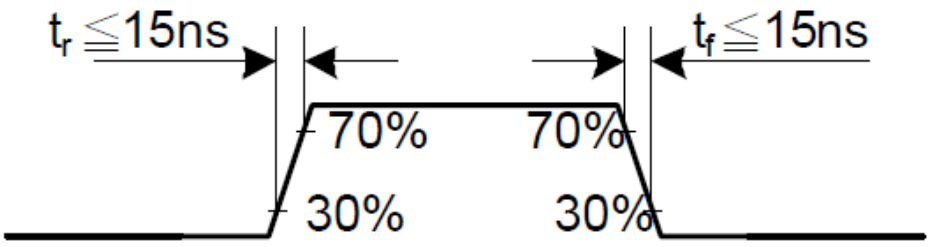
Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

7.2 Parallel 18/16/9/8-bit Timing (8080-I system)

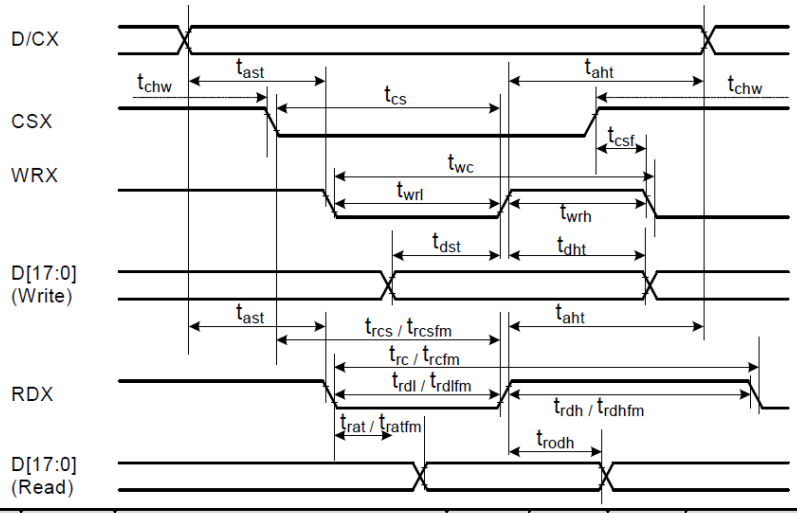


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: VCC=2.5 to 3.3V, GND=0V

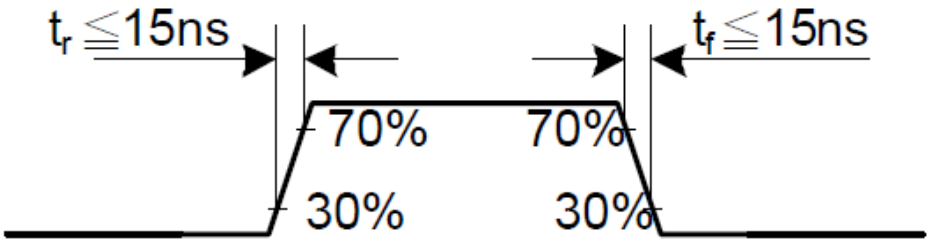


7.3 Parallel 18/16/9/8-bit Timing (8080-Ⅱ system)

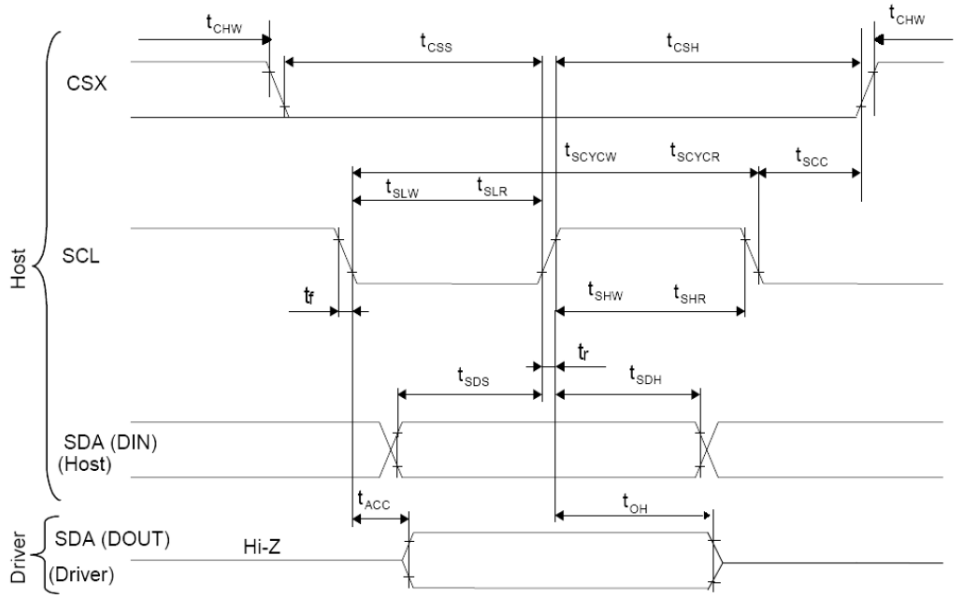


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: VCC=2.5 to 3.3V, GND=0V

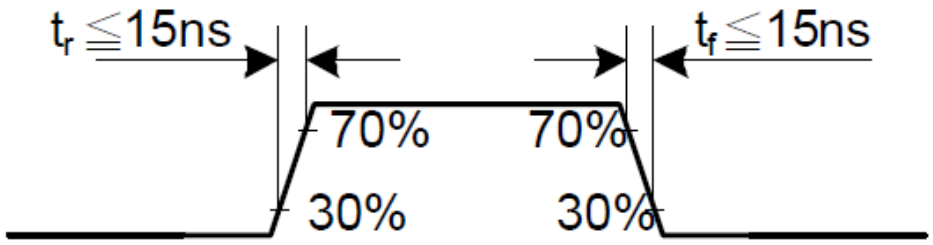


7.4 Display Serial Timing (3-line SPI system)

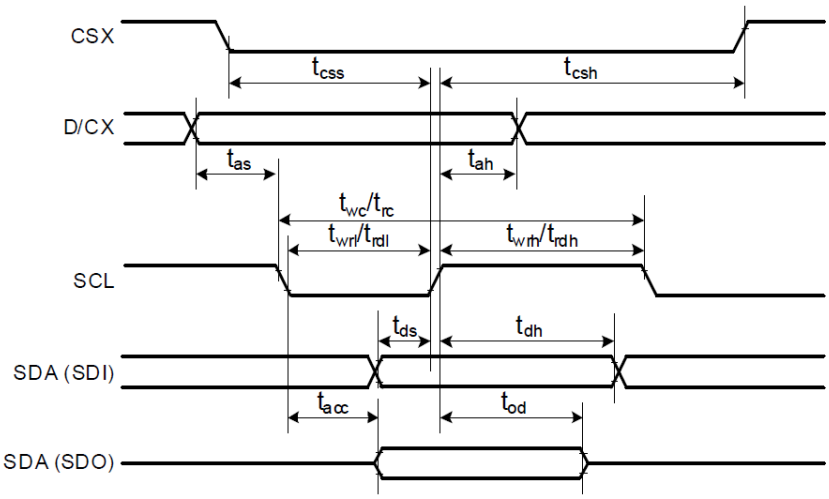


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: VCC=2.5 to 3.3V, GND=0V

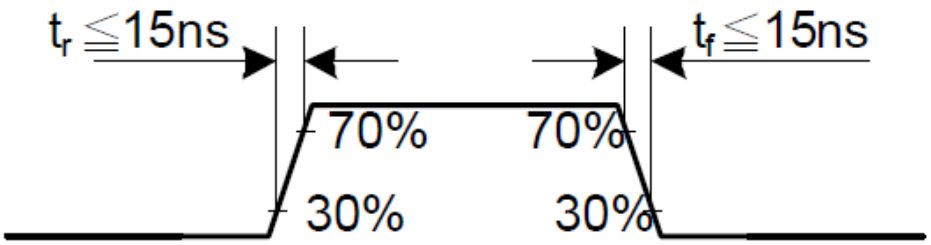


7.5 Display Serial Timing (4-line SPI system)

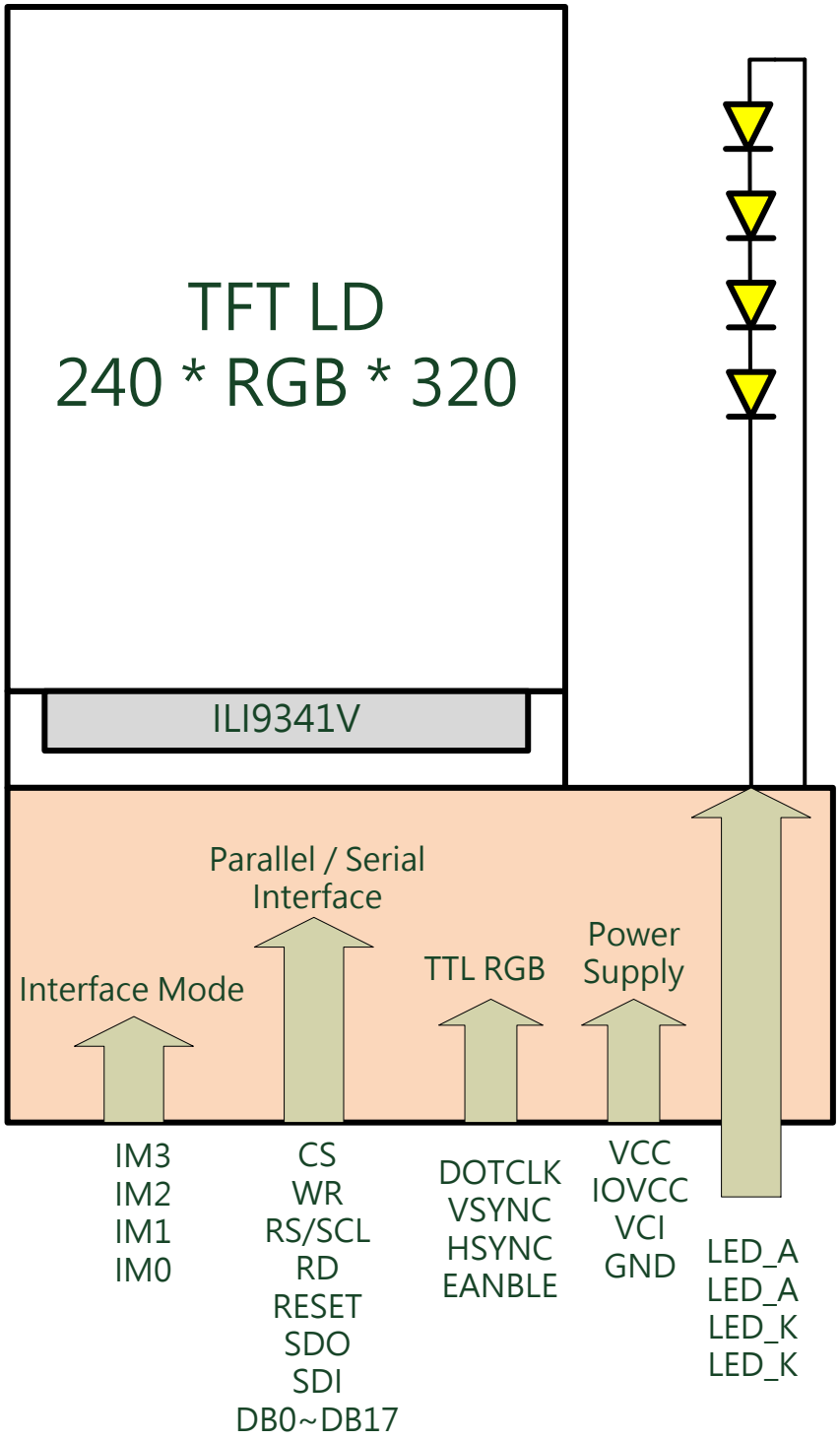


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: VCC=2.5 to 3.3V, GND=0V



7 BLOCK DIAGRAM



9 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	60±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	70±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2
Thermal Shock Test	-20°C (30min) ~ 70°C (30min) 100 cycles	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35℃ , 45-65%RH).

Note 3 : The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note 4 : All the reliability tests should be done without protective film on the module.

10 USE PRECAUTIONS

10.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

10.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light

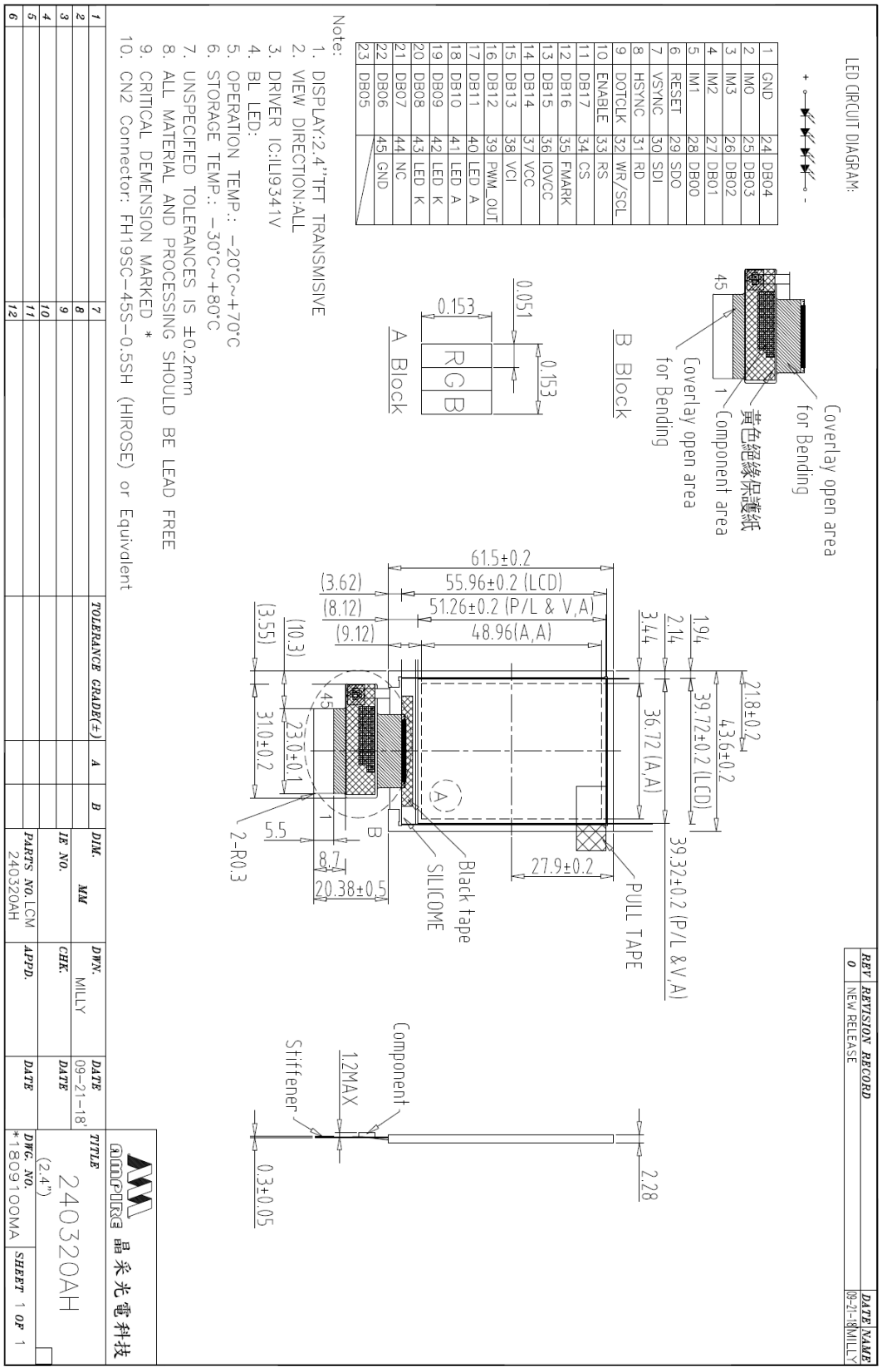
emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

10.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

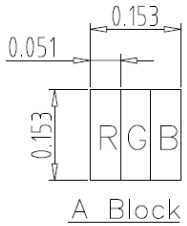
11 MECHANIC DRAWING



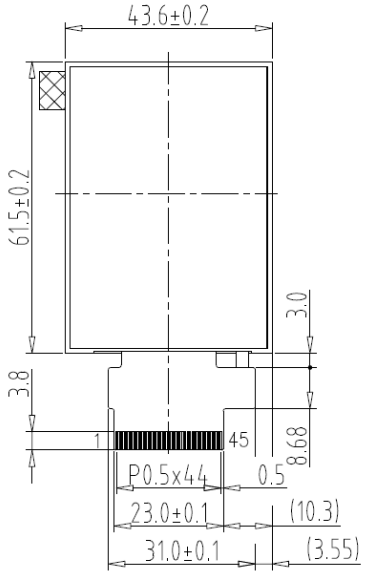
REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	09-21-18	MILLY

LED CIRCUIT DIAGRAM:

1	GND	24	DB04
2	IM0	25	DB03
3	IM3	26	DB02
4	IM2	27	DB01
5	IM1	28	DB00
6	RESET	29	SDO
7	VSYNC	30	SDI
8	HSYNC	31	RD
9	DOTCLK	32	WR/SCL
10	ENABLE	33	RS
11	DB17	34	CS
12	DB16	35	FMARK
13	DB15	36	IOVCC
14	DB14	37	VCC
15	DB13	38	VCI
16	DB12	39	PWM_OUT
17	DB11	40	LED A
18	DB10	41	LED A
19	DB09	42	LED K
20	DB08	43	LED K
21	DB07	44	NC
22	DB06	45	GND
23	DB05		



A Block



Note:

1. DISPLAY:2.4''TFT TRANSMISIVE
2. VIEW DIRECTION:ALL
3. DRIVER IC:ILI9341V
4. BL LED:
5. OPERATION TEMP.: −20°C~+70°C
6. STORAGE TEMP.: −30°C~+80°C
7. UNSPECIFIED TOLERANCES IS ±0.2mm
8. ALL MATERIAL AND PROCESSING SHOULD BE LEAD FREE
9. CRITICAL DEMENSION MARKED *
10. CN2 Connector: FH19SC−45S−0.5SH (HIROSE) or Equivalent

AMPIRE 晶采光電科技

				TOLERANCE GRADE(±)	A	B	DIM. MM	DWN. MILLY	DATE 09-21-18'	TITLE 240320AH (2.4")
1		7								
2		8								
3		9					IE NO.	CHK.	DATE	
4		10								
5		11					PARTS NO. LCM 240320AH	APPD.	DATE	DWG. NO. *1809101MA
6		12								SHEET 1 OF 1